CLAIMS

1. A memory cell structure comprising:

a semiconductor substrate;

a first silicon oxide layer situated over said semiconductor substrate;

a charge storing layer situated over said first silicon oxide layer, said charge storing layer comprising silicon nitride having reduced hydrogen content, said reduced hydrogen content reducing charge loss in said charge storing layer;

a second silicon oxide layer situated over said charge storing layer;

a gate layer situated over said second silicon oxide layer.

2. The memory cell structure of claim 1, further comprising:

said first silicon oxide layer, said charge storing layer, said second silicon oxide layer, and said gate layer forming a gate stack, said gate stack having a sidewall;

a spacer adjacent to said sidewall of said gate stack, said spacer comprising silicon nitride having reduced hydrogen content, said reduced hydrogen content reducing charge loss in said charge storing layer.

3. The memory cell structure of claim 2, wherein said gate stack is situated over a channel region in said semiconductor substrate, said channel region situated between a first terminal region and a second terminal region.

4. The memory cell structure of claim 1, wherein said charge storing layer has a

hydrogen content less than 1.0 atomic percent.

5. The memory cell structure of claim 1, wherein said charge storing layer has a hydrogen content between 0 and 0.5 atomic percent.

6. The memory cell structure of claim 1, wherein said charge storing layer is capable of storing two bits.

7. The memory cell structure of claim 1, wherein said charge storing layer is formed from nitrogen radicals.

8. A method for fabricating a memory cell structure, said method comprising:

providing a semiconductor substrate;

forming a first silicon oxide layer over said semiconductor substrate;

providing a precursor comprising a combination of silane and reactive nitrogen;

forming said silicon nitride layer over said first silicon oxide layer using said precursor in a CVD process.

9. The method of claim 8, wherein said CVD process is carried out at a temperature between 400 and 650° C.

10. The method of claim 8, further comprising annealing said silicon nitride layer

in an ambient of oxygen or nitrous oxide.

11. The method of claim 10, wherein said annealing is carried out at a temperature between 900 and 1000° C.

12. The method of claim 8, further comprising:

forming a second silicon oxide layer over said silicon nitride layer; and

forming a gate layer over said second silicon oxide layer.

13. The method of claim 8, wherein said reactive nitrogen comprises nitrogen radicals.

14. A memory cell structure comprising:

a semiconductor substrate, a first silicon oxide layer situated over said semiconductor substrate, a charge storing layer situated over said first silicon oxide layer, a second silicon oxide layer situated over said charge storing layer, a gate layer situated over said second silicon oxide layer, said memory cell structure characterized by:

said charge storing layer comprising silicon nitride having reduced hydrogen content;

said reduced hydrogen content reducing charge loss in said charge storing layer.

15. The memory cell structure of claim 14, further comprising:

said first silicon oxide layer, said charge storing layer, said second silicon oxide layer, and said gate layer forming a gate stack, said gate stack having a sidewall;

a spacer adjacent to said sidewall of said gate stack, said spacer comprising silicon nitride having reduced hydrogen content, said reduced hydrogen content reducing charge loss in said charge storing layer.

16. The memory cell structure of claim 14, wherein said gate stack is situated over a channel region in said semiconductor substrate, said channel region situated between a first terminal region and a second terminal region.

17. The memory cell structure of claim 14, wherein said charge storing layer has a hydrogen content less than 1.0 atomic percent.

18. The memory cell structure of claim 14, wherein said charge storing layer has a hydrogen content between 0 to 0.5 atomic percent.

19. The memory cell structure of claim 14, wherein said charge storing layer is capable of storing two bits.

20. The memory cell structure of claim 14, wherein said charge storing layer is

formed from nitrogen radicals.